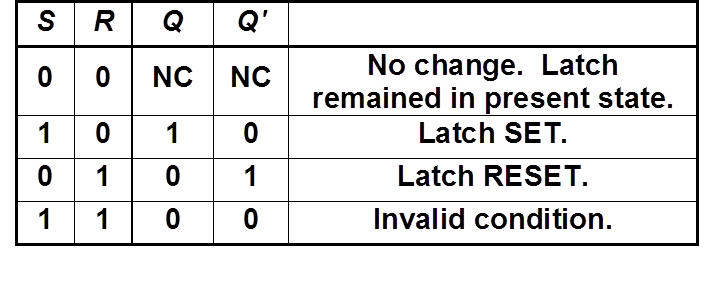
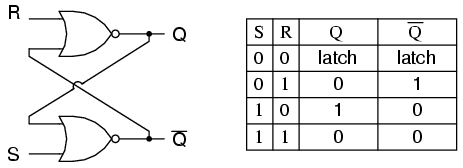
**Circuit Diagram & Truth Table:**

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**Code:**

* **Design Module**

modulers(q,qb,r,s);

inputr,s;

outputq,qb;

nor n1(q,r,qb);

nor n2(qb,s,q);

endmodule

* **TestBench**

module tb;

regr,s;

wireq,qb;

rsrsl(q,qb,r,s);

initial

begin

r=1'b0;s=1'b0;

#30

r=1'b0;s=1'b1;

#30

r=1'b1;s=1'b0;

#30

r=1'b1;s=1'b1;

#30

$finish;

end

endmodule